REMARKS

Claims 16-24 and 33-43 are pending in the present application. Claims 1-15 and 25-32 are canceled. Claims 16-18, 33, 35, and 36 are amended. More particularly, claims 18 and 35 are amended to be placed in independent form, since claims 18-24 and 35 are allowable over the prior art. Claims 37-43 are added. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to clarify the specification. No new matter is added by any of the amendments to the specification.

I. 35 U.S.C. § 112, First Paragraph

The Office Action rejects all pending claims under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to all pending claims, the Office Action states:

> It is unclear from the specification how figures 4, 5,7,8,9 are interconnected and associated with each other. Therefore the operation of these figures are not well understood.

Office Action, dated May 22, 2003. Applicant respectfully disagrees. It is clear from the specification that **Figures 4, 5, 7, 8,** and 9 illustrate varying views and embodiments of the present invention. For example, **Figure 4** depicts a wafer, while **Figure 5** illustrates a reticle (a contiguous group of integrated circuits on a wafer that were manufactured at the same time) and **Figure 6** depicts a single integrated circuit. These figures are not intended to be "interconnected," as stated in the Office Action.

Figure 7 is a block diagram describing the operation of a self test. The description of **Figure 7** clearly states that pseudo random sequences of bits may be applied to a main circuit through the use of a linear feedback shift register. **Figure 8** illustrates an example linear feedback shift register. The description of **Figure 7** also clearly states that a results comparator may calculate a signature value based on the results of the main circuit through the use of a multi-input signature register. **Figure 9**

illustrates an example multi-input signature register. A person of ordinary skill in the art would certainly know how these figures are interconnected or associated with one another, particularly by the description provided in the present invention.

Therefore, the present specification does indeed describe the claimed invention in such a way as to enable a person of ordinary skill in the art to make and use the claimed invention without undue experimentation. Thus, the rejection is improper and should be withdrawn.

II. 35 U.S.C. § 102, Anticipation

The Office Action rejects claims 16 and 17 under 35 U.S.C. § 102 as being anticipated by *Tomita* (US Patent No. 5,270,655). This rejection is respectfully traversed.

With respect to claims 16, 17, and 32, the Office Action states:

> As to claim 16, Tomita discloses in figure 3 a semiconductor apparatus having a test circuitry (38) and a plurality of similar circuit components (integrated circuits (32, 33, 34, 35)). It appears that each of the circuit components connected to testing circuitry (38). According to Tomita, the input/output pads of each of the circuit components are tested concurrently by the test circuitry (38) (see column 7, lines 23-42) and this test circuitry (38) would indicate if there are some defects by lighting up the LED (see column 7, lines 23-42).
>
> As to claim 17, it appears that the circuit components connected to the test circuitry (38) and this circuitry (38) includes a visible subcomponent (LED).

Office Action, dated May 22, 2003. Applicant respectfully disagrees. *Tomita* teaches a semiconductor integrated circuit having light emitting devices. An integrated circuit includes an internal main function circuit 42, a test circuit 43, and a plurality of light emitting devices 44. The test circuit tests the functions of the internal main circuit. Test results are output through the light emitting devices. See col. 7, line 57, to col. 8, line 16.

In contradistinction, the present invention provides an apparatus and method for automatically and permanently marking integrated circuits on at the wafer level. Claim 16, as amended, recites:

> 16. A wafer for testing by a testing device, the wafer comprising:
> a plurality of integrated circuits, wherein each integrated circuit includes testing circuitry;

a network of signal paths on the wafer, wherein the network of signal paths connects the plurality of integrated circuits to two or more connection points,

wherein in response to the testing device being connected to the connection points, the testing circuitry performs a test on the plurality of integrated circuits concurrently, and

wherein each integrated circuit includes at least one visible component having an appearance and wherein the at least one visible component permanently changes its appearance in response to failing the test.

Tomita does not teach or suggest a wafer for testing by a testing device having a plurality of integrated circuits, wherein each integrated circuit on the wafer includes testing circuitry and at least one visible component, and a network of signal paths on the wafer for connecting the plurality of integrated circuits to two or more connection points. *Tomita* also fails to teach or suggest a testing device being connected to the connection points and performing a test on the plurality of integrated circuits **concurrently**. Furthermore, since *Tomita* teaches light emitting devices, *Tomita* fails to teach or suggest the at least one visible component **permanently** changes its appearance in response to failing the test.

The applied reference fails to teach or suggest each and every claim limitation. Therefore, claim 16 is not anticipated by *Tomita*. Since claim 17 depends from claim 16, the same distinctions between *Tomita* and the invention recited in claim 16 apply for this claim. Additionally, claim 17 recites other additional combinations of features not suggested by the reference.

Therefore, the rejection of claims 16-17, 25, 29 and 32 under 35 U.S.C. § 102 has been overcome.

Furthermore, *Tomita* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Tomita* actually teaches away from the presently claimed invention because it teaches a light emitting device, which only indicates the status of an integrated circuit while the integrated circuit is in operation, as opposed to an apparatus for automatically and permanently marking an integrated circuit on a wafer, as in the presently claimed invention. Absent the Office Action pointing out some teaching or incentive to implement *Tomita* to concurrently test all integrated circuits on a wafer and to permanently mark an integrated circuit, one of

ordinary skill in the art would not be led to modify *Tomita* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Tomita* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicant's disclosure as a template to make the necessary changes to reach the claimed invention.

The Office Action rejects claims 33-34, and 36 under 35 U.S.C. § 102 as being anticipated by *Dukes et al.* (US Patent No. 5,570,035). This rejection is respectfully traversed.

With respect to claims 33, the Office Action states:

> As to claims 1-3, 25-26, 28-29 and 33, Dukes et al disclose in figure 2 an apparatus having at least one integrated circuit (34, 36, 38, 40) and a visible circuit component (26) associated with one of the integrated circuit (34, 36, 38, 40).

Office Action, dated May 22, 2003. Applicant respectfully disagrees. *Dukes* provides a built-in self test indicator for an integrated circuit package. An integrated circuit or multi-chip module includes a built-in self test and a visible indicator. See FIGS. 1 and 2.

Claim 33, as amended, recites:

> 33. A method of testing a circuit, comprising:
> connecting a testing device to connection points on a wafer, wherein the wafer has fabricated thereon a plurality of integrated circuits and wherein each integrated circuit within the plurality of integrated circuits includes a testing circuit and a visible circuit component;
> applying at least one signal to each testing circuit concurrently;
> in response to a determination that an integrated circuit from within the plurality of integrated circuits is defective, modifying the visible circuit component in the defective integrated circuit to permanently change appearance.

Dukes does not teach "connecting a testing device to connection points on a wafer, wherein the wafer has fabricated thereon a plurality of integrated circuits and wherein each integrated circuit within the plurality of integrated circuits includes a testing circuit and a visible circuit component" and "applying at least one signal to each testing circuit concurrently," as recited in claim 33.

The applied reference fails to teach or suggest each and every claim limitation. Therefore, claim 33 is not anticipated by *Dukes*. Since claims 34 and 36 depend from

claim 336, the same distinctions between *Dukes* and the invention recited in claim 33 apply for these claims. Additionally, claims 34 and 36 recite other additional combinations of features not suggested by the reference.

Therefore, the rejection of claims 33, 34, and 36 under 35 U.S.C. § 102 is overcome.

Furthermore, *Dukes* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Dukes* actually teaches away from the presently claimed invention because it is primarily concerned with monitoring parts while they are active or in operation (see col. 2, lines 39-43), as opposed to a method for automatically and permanently marking an integrated circuit on a wafer, as in the presently claimed invention. Absent the Office Action pointing out some teaching or incentive to implement *Dukes* to concurrently test all integrated circuits on a wafer and to permanently mark an integrated circuit, one of ordinary skill in the art would not be led to modify *Dukes* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Dukes* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicant's disclosure as a template to make the necessary changes to reach the claimed invention.

III. Conclusion

It is respectfully urged that the subject application is patentable over *Tomita* and *Dukes* and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: August 22, 2003

Respectfully submitted,

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